LPC Module

Summary

The Low Pin Count (LPC) module is the interface which is used to communicate information between TPM and PC (through one PC to TPM Bridge). It meets the TCG TPM V1.2 Interface Specification, and is compatible with TCG TPM V1.1b at the same time.

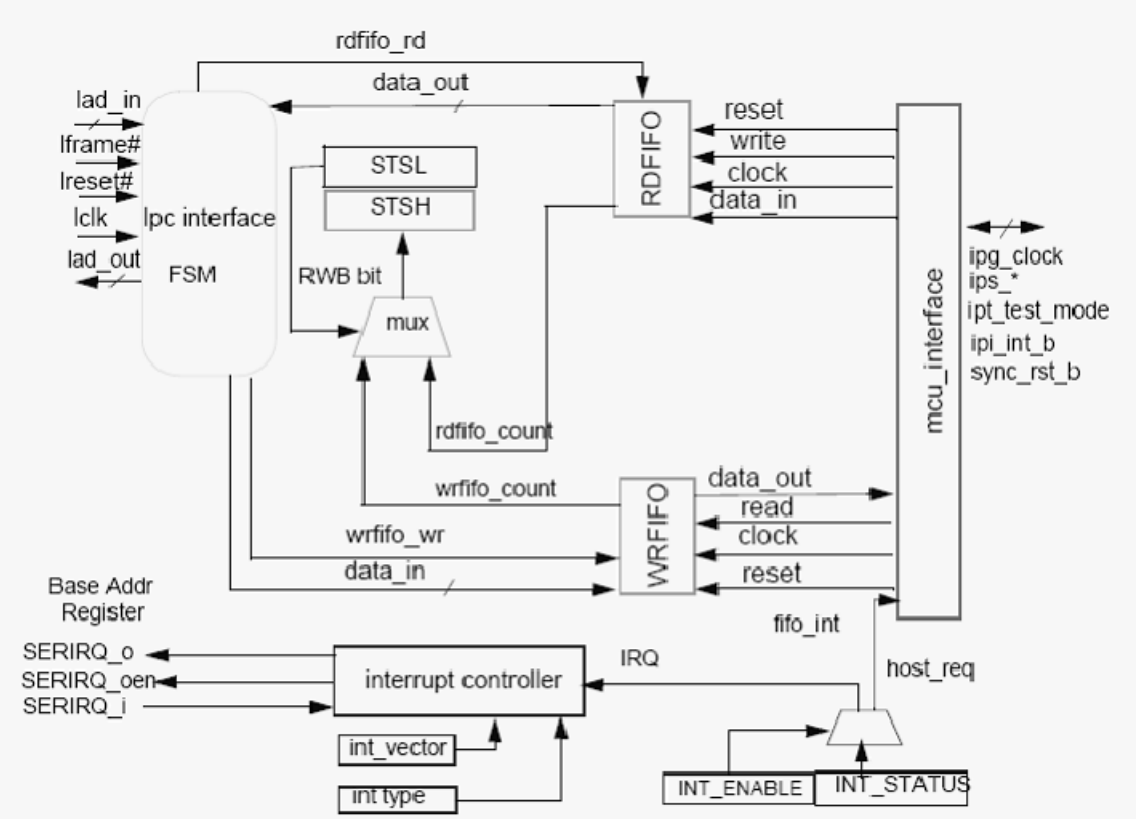

Figure 16-1 LPC Block Diagram

LPC Block Diagram

Signal Description

Name	Direction	Function	Pullup
LAD[3:0]	I/O	Data, address, command bus	YES
LFRAME#[1]	I	Indicated start of a new cycle, termination of broken cycle	YES
LRESET#	I	reset, same as the PCI reset on the host	YES
LCLK	I	clock: same 33MHz clock as PCI clock on the host.	-
SERIRQ#	I/O	Interrupt request	YES
LPCPD#	I	Indicates taht the peripheral should prepare for power to be removed from the LPC I/F devices.	YES
PP	I	Physical present signal	PULL Down
BADDR[1:0]	I	Configuration Inputs for CFGL Register	YES

To obtain more information about the LPC *or other C*Core™ products, please contact the C*Core Technology Co., Ltd. by phone: 0512-68091377, email: support@china-core.com or web: http://www.china-core.com.*

*C*Core™ is a trade mark of C*Core Co., Ltd.*