CCFC2006PT
Datasheet
Rev 0.0

HCMOS
Microcontroller Unit

IC Design Group
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Revision History

Release Number	Date	Author	Summary of Changes
0.0	2017.6.24	hwliu	Original version

Section 1 Overview

1.1 Introduction

CCFC2006PT is a chip based on C2006 PowerPC processor. The C2006 CPU is part of the family of CPU cores that implement versions builton the Power Architecture embedded category. This core also has additional instructions, including digitalsignal processing (DSP) instructions, beyond the classic PowerPC instruction set.

CCFC2006PT has two lelvels of memory hierarchy.the fastest accesses are to the unified cache(32KB). The next level in the hierarchy contrains the 64-kByte internal SRAM and internal flash memory(2MB). Both the internal SRAM and flash memory can hold instructions and data. The external bus interface has designed to support most of the standard momories.

The Complex I/O timer functions of the CCFC2006PT are perfromed by two enhanced time processor unit eTPU. Each eTPU engine conrols 32 hardware channels. The eTPU has been enhanced over the TPU by providing 24-bit timers,double action hardware channels. variable number of parameter per channel, angle clock hardware , and additional control and arithmetic instructions. Th eTPU can be programmed using a high-level programming language.

The less complex timer functions of CCFC2006PT are perfromed by enhanced modular input/output system(eMIOS). The eMIOS'24 hardware channels are capable of single action, double action,pluse width modulation(PWM) and modulus counter operation. Motor control capabilities include edge-aligned and center-alignd PWM.

Off-chip communication is performed by a suite of serail protocols including controller area networks(three FlexCANs) , an enhanced deserial/serial peripheral interface(four DSPI), and endhanced serial communications interfaces(eSCIs). The DSPIs support pin reduction through hardware serialization and deserailization of timer channels and general-purpose input/output(GPIO) signals

The MCU of the CCFC2006PT has on-chip 40-channel enhanced queued dual analog to digital converter(eQADC).

The system integration unit(SIU)perfroms several chip-wide configuration functions.Pad coinfiguration and general-purpose input and output (GPIO) are controlled from the SIU. External interrupts and reset control are also found in the SIU. The internal multiplexer submodule(SIU_DISR)provide multiplexing of eQADC trigger sources, daisy chaining the DSPIs, and external interrupt signal multiplexing.

CCFC2006PT also has a DMA controller.

CCFC2006PT is designed for dynamic power management of core and peripherals. Software can controll the clock gating of peripherals.

1.2 Key Features

The following lists an overview of CCFC2006PT key feature set:

- Operation Parameters
  - Up to **132**MHz operation frequency
  - –40 °C to 150°C junction temperature operating range
  - Low power design
    - Designed for dynamic power management of core and peripherals
    - Software power supply for stand-by operation for portion of internal SRAM
  - Fabricate in 0.13um process
  - 1.5V internal logic
  - Input and output pins with 3.0V-5.5V range
    - 35%/65% V_{DDE}CMOS swithch levels(with hysteresis)
    - Selectable hysteresis
    - Selectable Slew rate control
  - External bus and Nexus pins support 1.62V-3.6V operation
    - Selectable drive strength control
    - Unused pins configurable as GPIO
  - Designed with EMI reduction techniques
    - Frequency modulated phase-lock loop
    - On-chip bypass capacirance
    - Selectable Slew rate and drive strength
- High performance C2006 core processor
  - 32-bit CPU built on Power Architecture?
  - Thirty-two 64-bit general-purpose registers (GPRs)
  - Memory management unit (MMU) with 32-entry fully-associative translation look-asidebuffer (TLB)
  - Branch processing unit
  - Fully pipelined load/store unit
  - 32 kilobyte unified cache withline locking
    - 8-way set associative
    - Two 32-bit fetches per clock
    - 8-entry store buffer

    - Way locking
    - Supports assigning cache as instruction or data only on a per way basis
    - Supports tag and data parity
  - Vectored interrupt support
  - Interrupt latency < 70 ns @132MHz (measured from interrupt request to execution of first instruction of interrupt exception handler)
  - Reservation instructions for implementing read-modify-write constructs (internal SRAM andflash)
  - Signal processing engine (SPE) auxiliary processing unit (APU) operating on 64-bit GPRs
  - Floating point
    - IEEE 754 compatible with software wrapper
    - Single precision in hardware, double precision with software library
    - Conversion instructions between single precision floating point and fixed point
  - Long cycle time instructions, except for guarded loads, do not increase interrupt latency in the CCFC2006PT. To reduce latency, long cycle time instructions are aborted upon interrupt requests.
  - Extensive system development support through Nexus debug module
- System bus crossbar switch (XBAR)
  - 3 master ports
  - 5 slave ports
  - 32-bit address, 64-bit data paths
  - Simultaneous accesses from different masters to different slaves (there is no clock penaltywhen a parked master accesses a slave)
- Enhanced direct memory access (eDMA) controller
  - 64 channels support independent 8-, 16-, 32-, or 64-bitsingle value or block transfers.
  - Supports variable sized queues and circular queues.
  - Source and destination address registers are independently configured to post-increment orremain constant
  - Each transfer is initiated by a peripheral, CPU, or eDMA channel request.
  - Each eDMA channel can optionally send an interrupt request to the CPU on completion of asingle value or block transfer.
- Interrupt controller (INTC)

  - 308 total interrupt vectors
    - 278 peripheral interrupt requests
    - plus 8 software setable sources
    - plus 22 reserved interrupts
  - Unique 9-bit vector per interrupt source
  - 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
  - Priority elevation for shared resources
- Frequency modulated phase-locked loop(FMPLL)
  - Input clock frequency from 8MHZ to 20MHZ
  - Current controlled oscillator(ICO) range from 50MHZ mzximum device frequency
  - Reduced frequency divider(RFD) for reduced frequency operation without re-lock
  - Four selectable modes of operation
  - Programmable frequency modulation
  - Lock detect circuitry continuously monitors lock status
  - Loss of clock(LOC)detection for reference and feedback clocks
  - Self-clocked mode(SCM) operation
  - On-chip loop filer(reduces number of external components required)
  - Engineering clock output
- EBI
  - 1.8V-3.3V nominal I/O voltage
  - Memory controller with support for various memory types
  - 32bit data bus, 24 bit address bus with transfer size indication
  - Selectable drive strengths through padd control in SIU
  - Configurable bus speed modes
  - Support for external master accesses to internal addresses
  - Burst support
  - Bus monitor
    - User selectable
    - Programmable timeout period(with 8 external bus clock resolution)
  - Chip selects

    - Four chip select ($\overline{CS}$[0:3]) signals
  - Configurable wait states
- System integration unit (SIU)
  - Centralized GPIO control of 214 I/O and bus pins
  - Centralized pa control on a per-pin basis External interrupts
  - System reset monitoring and generation
  - External interrupt inputs,filtering and control
  - Internal multiplexer submodule(SIU_DISR,SIU_ETISR,SIU_EIISR)
- ECSM
  - Configurable error-correcting codes(ECC) reportting for internal SRAM and flash memories.
  - Program-visible information on the device configuration and revision
  - Registers for capturing information on memory errors due to error-correction codes
  - Registers to specify the generation of single- and double-bit memory data inversions for test purposes to check ECC protection
- On-chip flash
  - 2 Mbytes burst flash memory
  - 256K x 64-bit configuration
  - Censorship protection scheme to prevent flash content visibility
  - Hardware read-while-write feature that allows blocks to be erased/programmed while otherblocks are being read (used for EEPROM emulation and data calibration)
  - 20 blocks with sizes ranging from 16 Kbytes to128 Kbytes to support features such as boot block, operating system block, and EEPRO Memulation
  - Read while write with multiple partitions
  - Page programming mode to support rapid end of line programming
  - Hardware programming state machine
- CACHE Memory
  - 32 Kbyte cache memory
  - 8-wayset-associative unified(instruction and data) cache
- Internal SRAM
  - Total 64KBytes SRAM memory
  - Byte, halfword and word addressable

  - ECC (error correction code) protected with single-bit correction and double-bit detection
- BAM
  - Enables and managers the transition of MCU from reset to user code execution in the following configurations:
    - User application can boot from internal or external flash memory
    - Download and execution of the code via FlexCAN for eSCI.
- eMIOS
  - 24 channels with orthogonal channels with double action,PWM,and modulus counter functionality
  - four selectable time base plus shared time or angle counter bus
  - DMA and interrupt request support
    - Motor control capability
- eTPU
  - CCFC2006PT has two eTPU engines.
  - Each eTPU engine is an event_triggered timer subsystem
  - High level assembler/complier
  - 32 channels per engine
  - 24-bit timer resolution
  - 16Kbyte shared code memory in CCFC2006PT.
  - 3Kbyte shared data memory
  - Variable number of parameters allocatable per channel
  - Double match/capture channels
  - Angle clock hardware support
  - Shared time or angle counter bus for all eTPU and eMIOS modules
  - DMA and interruput request support
  - Nexus class 3 debug supoort(with some class 4 support)
- eQADC
  - 2 independent on-chip SAR ADCs
  - 8, 10, and 12-bit AD resolution
  - common mode conversion range (0–5V)

  - 40 signle-ended inputs channels, expandable to 65 channels with external multiplexers on 416 and 324 BGA package
  - 34 single-ended inputs channels, expandable to 57 channels with external multiplesers on 208 BGA packages
  - Eight channels can be used as four pairs of differential analog input channels
  - 10 bit accurauy at 400K Sample/s, 8 bit accuracy at 800K samples/s
  - Supports six CFIFOs with fixed priority. The lower the CFIFO number, the higher its priority. When commands of distinct CFIFOs are bound for the same CBuffer, the higher priority CFIFO is always served first.
  - Queue modes with priority-based preemption;initiated by software command, internal(eTPU and eMIOS),or external triggers
  - DMA and interrrupt request support
- DSPI x 4
  - SPI
    - Full-duplex communication ports with interrrupt and eDMA request support
    - Supports all functional modes from QSPI submodule of QSMCM
    - Support for queues in RAM
    - Six chip selects, expandable to 64 withexternal demultiplexers
    - Programmable frame size, baud rate, clock delay, and clock phase on a per-frame bais
    - Modified SPI mode for interfacing to peripherals with longer setup time requirements
  - Deserial serial interface(DSI)
    - Pin reduction by hardware serialization and deserialzation of eTPU and eMIOS channels
    - Chanining of DSI submodules
    - Triggered transfer control and change in data transfer control(for reduced EMI)
- eSCI x 2
  - UART mode provides NRZ format and half or full-duplex interface
  - eSCI bit reate up to 1Mbps
  - Advanced error detection, and optional parity generation and detection
  - word length programmable as 8 or 9 bits
  - Separately enabled transmitter and receiver
  - LIN support
  - DMA support
  - Interrrupt request support

- FlexCAN x 3
  - 64 message buffers each
  - Full implementation of the CAN protocol specification, Version 2.0B
  - Programmable acceptance filters
  - Short latency time for high priority transmit messages
  - Arbitration scheme according to message ID or message buffer number
  - Listen only mode capabilities
  - Programmable clock source: system clock or oscillator clock
- PIT
  - Support 4 channel with 32-bit width counter
  - Each timers can generate an individual interrupt request when timeout
  - Accessiable individual counter
  - Each channel can be controlled independently
  - Target value for each channel can be configured seperately
  - All interrupts are maskable
  - Independent timeout periods for each timer
- STM
  - One 32-bit up counter with 8-bit prescaler
  - Four 32-bit compare channels
  - Independent interrupt source for each channel
  - Counter can be stopped in debug mode
- SWT
  - 32-bit time-out register to set the time-out period
  - The unique SWT counter clock is the undivided slow internal RC oscillator 128 kHz (SIRC), no other clock source can be selected
  - Programmable selection of window mode or regular servicing
  - Programmable selection of reset or interrupt on an initial time-out
  - Master access protection
  - Hard and soft configuration lock bits

  - The SWT is started on exit of power-on phase (RGM phase 2) to monitor flash boot sequence phase. It is then reset during RGM phase3 and optionally enabled when platform reset is released depending on value of flash user option bit 31 (WATCHDOG_EN).
- Nexus development interface (NDI)
  - Per IEEE-ISTO 5001-2003
  - Real time development support for power ArchArchitecture core and eTPU engines through Nexus class 3 (some Class 4 support)
  - Data trace of eDMA accesses
  - Read and write access
  - Configured via the IEEE1149.1 (JTAG) port
  - High bandwidth mode for fast message transmission
  - Reduced bandwidth mode for reduced pin usage
- IEEE1149.1 JTAG controller (JTAGC)
  - IEEE 1149.1-2001 test access port (TAP) interface
  - A JCOMP input that provides the ability to share the TAP. Selectable modes of operation include JTAGC/debug or normal system operation.
  - A 5-bit instruction register that supports IEEE 1149.1-2001 defined instructions.
  - A 5-bit instruction register that supports additional public instructions.
  - Three test data registers: a bypass register, a boundary scan register, and a device identification register.
  - A TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry.
- Voltage regulator controller
  - Provides a low cost solution to power the core logic. It reduces the number of power supplies required from the customer power supply chip.
- POR block
  - Provides initial reset condition up to the voltage at which pins (RESET) can be read safely. It does not guarantee the safe operation of the chip at specified minimum operating voltages.

1.3 Block Diagram

Figure 1-1 is a block diagram of the system view.

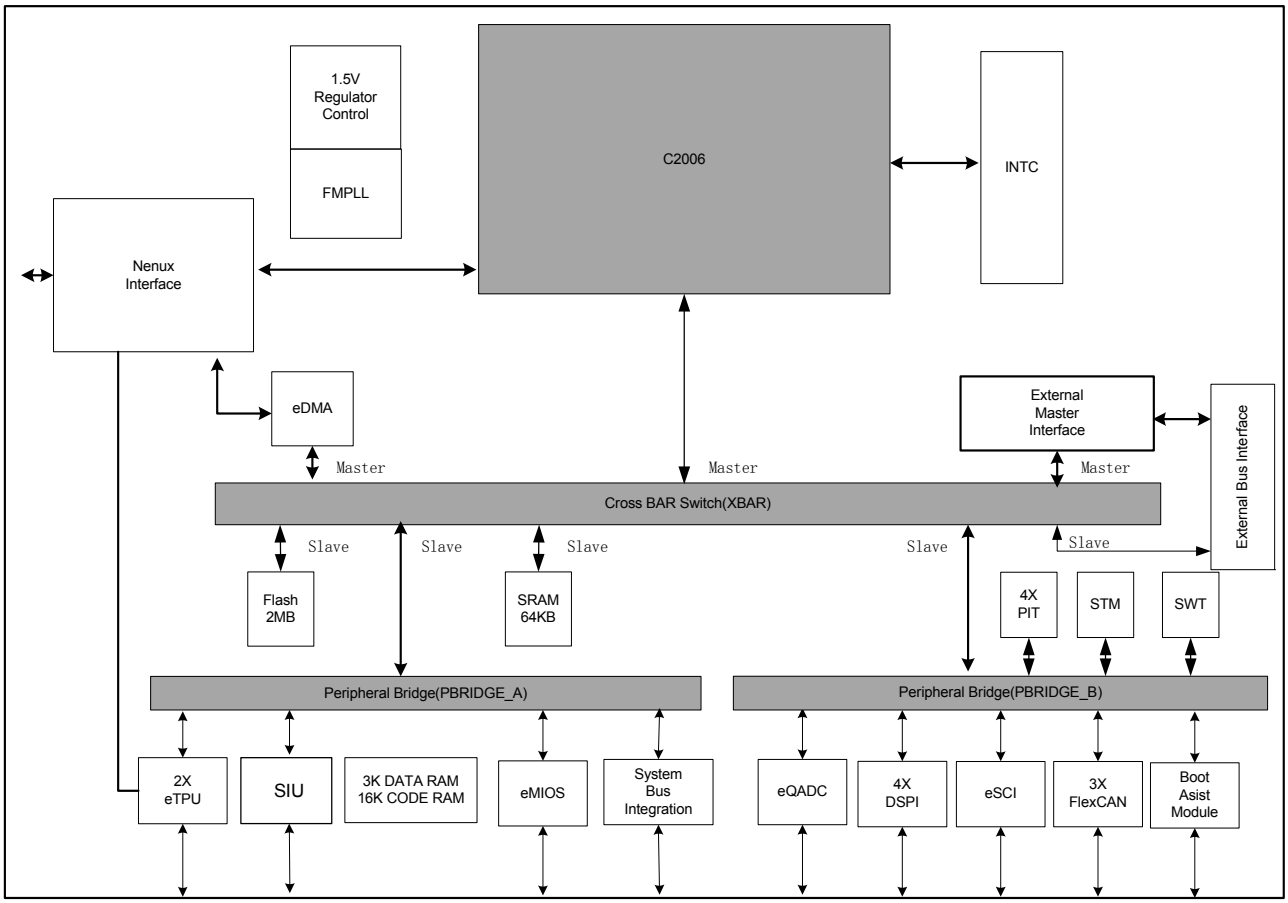

Figure 1-1 Block Diagram

Appendix A Preliminary Electrical Characteristic

A.1 General

This section provides electrical parametrics and electrical ratings for the CCFC2006PT microcontroller unit.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle; however, for production silicon these specification will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

A.2 Absolute Maximum Ratings

Maximum ratings are the extreme limits to which the MCU can be exposed without permanently damaging it. See **Table A-1**.

The MCU contains circuitry to protect the inputs against damage from high static voltages; however, do not apply voltages higher than those shown in the table. Connect unused inputs to the appropriate voltage level, either V_{SSH} and V_{DDH}. This device is not guaranteed to operate properly at the maximum ratings.

Table A-1 Absolute Maximum Ratings

Num	Rating	Symbol	Value	Unit
1	IO Supply Voltage	V_{DD5V}	-0.5 to +6.0	V
2	Core Supply Voltage	V_{DD}	-0.5 to +1.65	V
3	Input Voltage[1]	V_{IN}	-0.3 to +6.0	V
4	Injected input current on any pin during overload condition	I_D	-10 to 10	mA
5	Operating temperature range	T_{OPT}	-40 to +150	^{O}C
6	Storage temperature range	T_{STG}	-55 to +150	^{O}C

NOTES:

1. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

A.3 Electrostatic Discharge (ESD) Protection

Table A-2 ESD Protection Characteristics

Parameter[1,2]	Symbol	Value	Units
ESD target for human body model	HBM	2000	V
ESD target for charged device model	CDM	500	V
	CDM(corners)3	750	V

NOTES:

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temparature, unless specified otherwise in the device specification.

A.4 Power Management Electrical Characteristics

A.4.1 PMU Electrical Characteristics

Table A-3 PMU Electrical Characteristics

Symbol	Parameter	Vaule			Unit
		Min	Typ	Max	
3.3V LDO					
V_{dd}	Input Supply Voltage	3.6	5.0	6.0	V
V_{REG}	Regulator Output Voltage		3.3		V
I_{REG}	Regulator Output Current		80	100	mA
t_{REG}	Regulator Power up Time		100		μs
I_{CONS}	Regulator Current Consumption		8.5		μA
C_{REG}	Regulator External Ceramic capacitance	0.47	1	2.2	μF
R_{REG}	Regulator Equivalent Series Resistance (ESR)	5		300	mΩ
Low voltage detector					
V_{TH1P5V}	External 1.5V LDO LVD input supply voltage voltage threshold		1.5		V
$V_{HYS1P5V}$	External 1.5V LDO LVD V_{TH} hysterisis voltage		0.15		V

Table A-3 PMU Electrical Characteristics

V_{TH3P3V}	3.3V LDO LVD input supply voltage voltage threshold		2.8		V
$V_{HYS3P3V}$	3.3V LDO LVD V_{TH} hysterisis voltage		0.2		V
$V_{THavdd3P3V}$	5.0V supply voltage LVD input supply voltage voltage threshold		2.8		V
$V_{HYSavdd3P3V}$	5.0V supply voltage LVD V_{TH} hysterisis voltage		0.2		V
$V_{THavdd5P5V}$	5.0V supply voltage LVD input supply voltage voltage threshold		4.4		V
$V_{HYSavdd5P5V}$	5.0V supply voltage LVD V_{TH} hysterisis voltage		0.2		V
1.5V Power on reset					
V_{dd}	Input Supply Voltage	1.35	1.5	1.65	V
V_{TH}	Supply Voltage Trip Threshold		0.9		V
3.3V Power on reset					
V_{dd}	Input Supply Voltage	2.2	3.3	6.0	V
V_{TH}	Supply Voltage Trip Threshold		1.65		V
5.0V Power on reset					
V_{dd}	Input Supply Voltage	2.2	5.0	6.0	V
V_{TH}	Supply Voltage Trip Threshold		1.7		V

A.4.2 Power-Up Sequence

The 1.5 V VDD power supply must rise to 1.35 V before the VDD5V power supply rises above 2.8 V. This ensures that digital logic in the PLL for the 1.5 V power supply does not begin to operate below the specified operation range lower limit of 1.35 V. The internal VDD5V POR will hold the device in reset as low as 2.8 V, VDD must be within specification before the VDD5V POR negate.

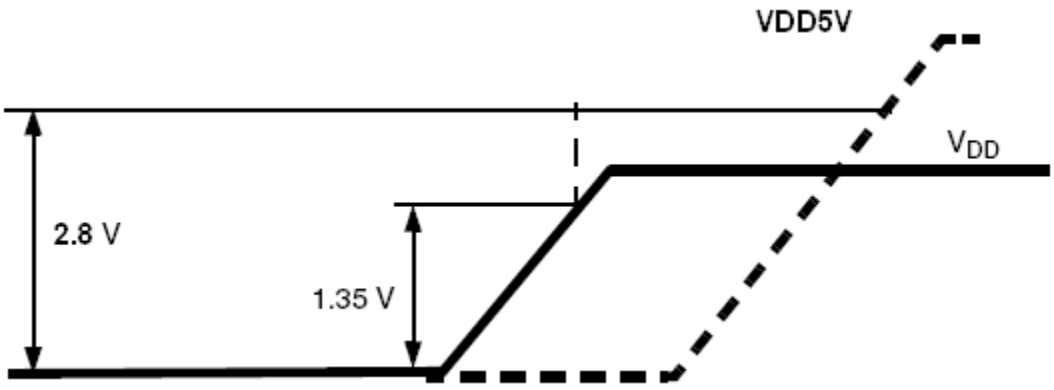

Figure A-1 Power-Up sequence

A.4.3 Power-Down Sequence

The only requirement for the power-down sequence with VDD5V grounded is if VDD decreases to less than its operating range(1.35V ~ 1.65V), VDD5V power must decrease to less than 2.8 V . This ensures that the digital 1.5 V logic, which is reset only by VDD5V POR and can cause the 1.5 V supply to decrease less than its specification value, resets correctly.

A.5 ADC Electrical Characteristics

Table A-4 ADC conversion characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
V_{DDA}	Analog supply voltage	2.7	3.3/5.0	5.5	V
V_{REFH}	Reference supply voltage high			V_{DDA}	V
V_{REFL}	Reference supply voltage low		0		V
V_{AIN}	Conversion voltage range	0		V_{REFH}	V
T_A	Temperature range			150	℃
f_{ADC}	ADC clock frequency			16	MHz
f_{CONV}	12-bit conversion rate			1	MS/s
$I_{ADCVREFH}$	ADC VREFH consumption in running mode		550		uA

Table A-4 ADC conversion characteristics

I_{ADCPWD}	ADC consumption in power down mode		1		uA
I_{ADCRUN}	ADC consumption in running mode		2		mA
t_{ADC_PU}	ADC power up delay		2		µs
t_s	Sampling time	3			clk
t_c	Conversion time		12		clk
C_S	ADC input sampling capacitance		6.4		pF
C_{P1}	ADC input pin capacitance		3		pF
DNL	Differential Nonlinearity (DNL)		±3		LSB
INL	Integral Nonlinearity (INL)		±8		LSB

Table A-5 ADC input leakage current

Symbol	Parameter	Conditions		Value			Unit
				Min	Typ	Max	
I_{LKG}	Input leakage current	T_A = - 150 °C	No current injection on adjacent pin	-2.5		2.5	uA

A.6 I/O pad electrical characteristics

A.6.1 I/O input DC characteristics

Table A-6 I/O input DC electrical characteristics

Symbol	Parameter	Conditions[1]		Value			Unit
				Min	Typ	Max	
V_{IH}	Input high level	V_{DD5V} = 5.0 V		0.65*VDD5V		VDD5V	V
V_{IL}	Input low level	V_{DD5V} = 5.0 V		VSS		0.35*VDD5V	
V_{HYS}	Input hysteresis	V_{DD5V} = 5.0 V			0.1*VDD5V		
I_{LKG}	Digital input leakage	No injection on adjacent	T_A = - 150 °C	-2.5		2.5	uA
I_{LOADD}	Digital IO input capitance	T_A = 25 °C				7	pF
I_{LOADC}	Analog/Digital IO input capitance	T_A = 25 °C				12	pF

NOTES:

1. T_A = - 40 to 150 °C, unless otherwise specified.

A.6.2 I/O output DC characteristics

Table A-7 I/O pull-up/pull-down DC electrical characteristics

Symbol	Parameter	Conditions[1]		Value			Unit
				Min	Typ	Max	
$\|I_{WPU}\|$	Weak pull-up current absolute value	$V_{IN} = V_{IL}$, V_{DD5V} = 5.0 V	pad_i_SPTP = 1	50		250	µA
$\|I_{WPD}\|$	Weak pull-down current absolute value	$V_{IN} = V_{IH}$, V_{DD5V} = 5.0 V	pad_i_SPTP = 1	50		250	µA

NOTES:

1. T_A = - 40 to 150 °C, unless otherwise specified.

Table A-8 Low Drive configuration output buffer electrical characteristics

Symbol	Parameter	Conditions[1]	Value			Unit
			Min	Typ	Max	
V_{OH}	Output high level low drive configuration	I_{OH} =5 mA, V_{DD5V} = 5.0 V, pad_i_SPTP = 1 (recommended)	0.8*VDD5V		VDD5V	V
V_{OL}	Output low level low drive configuration	I_{OL} = 5 mA, V_{DD5V} = 5.0 V, pad_i_SPTP = 1 (recommended)	0		0.1*VDD5V	V

NOTES:

1. T_A = - 40 to 150 °C, unless otherwise specified.

Table A-9 High Drive configuration output buffer electrical characteristics

Symbol	Parameter	Conditions[1]	Value			Unit
			Min	Typ	Max	
V_{OH}	Output high level High Drive configuration	I_{OH} = 10 mA, V_{DD5V} = 5.0 V, pad_i_SPTP = 1 (recommended)	0.8*VDD5V		VDD5V	V

Table A-9 High Drive configuration output buffer electrical characteristics

V_{OL}	Output low level High Drive configuration	I_{OL} = 10mA, V_{DD5V} = 5V , pad_i_SPTP = 1 (recommended)	0		0.1*VDD5V	V

NOTES:

1. T_A = - 40 to 150 °C, unless otherwise specified.

A.7 FMPLL Electrical Characteristics

A.7.1 FMPLL electrical characteristics

Table A-10 PLL electrical characteristics

Symbol	Parameter	Conditions[1]	Value			Unit
			Min	Typ	Max	
f_{PLLIN}	FMPLL reference clock[2]		8			MHz
f_{PLLOUT}	FMPLL output clock frequency		10M		500	MHz
f_{DUTY}	FMPLL output clock duty cycle		45	50	55	%
t_{LOCK}	FMPLL lock time	Stable oscillator (f_{PLLIN} = 16 MHz)		200		µs
Δt_{LTJIT}	FMPLL period jitter,RMS	@500MHz,T_A = 25 °C		10		ps
I_{PD}	FMPLL power-down consumption				10	uA

NOTES:

1. V_{DD5V} = 5.0 V ± 10%, T_A = - 40 to 150 °C, unless otherwise specified.
2. PLLIN clock retrieved directly from FXOSC clock. Input characteristics are granted when oscillator is used in functional mode.